CLAIMS

1. (Currently Amended) An apparatus for current leakage correction coupled to a leaky capacitor, wherein the leaky capacitor is connected to ground, comprising:

a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

a plurality of current mirrors, wherein the plurality of current mirrors further comprise:

at least one first current mirror is at least configured to be coupled to the leaky capacitor; and

at least one second current mirror is at least configured to be coupled to the scaled capacitor that is at least configured to provide a potential difference across the scaled capacitor that is substantially equal to a potential difference across the leaky capacitor minus the potential difference across the at least one second current mirror.

2. (Original) The apparatus of Claim 1, wherein the plurality of current mirror further comprises a plurality of transistors.

3. (Original) The apparatus of Claim 1, wherein the plurality of current mirrors further comprises a plurality of Field Effect Transistors (FET).

4. (Original) The apparatus of Claim 3, wherein at least one FET of the plurality of FETs is a Positive-Channel FET (PFET), wherein the PFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

5. (Original) The apparatus of Claim 4, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

6. (Original) The apparatus of Claim 3, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

7. (Original) The apparatus of Claim 1, wherein the plurality of current mirrors further comprise a plurality of bipolar transistors.

8. (Original) The apparatus of Claim 1, wherein the plurality of current mirrors further comprise a plurality of Metal-Oxide Semiconductor FETs (MOSFETs).

9. (Original) The apparatus of Claim 8, wherein at least one MOSFET of the plurality of MOSFETs is a Positive-type MOSFET (P-type MOSFET), wherein the P-type MOSFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

10. (Original) The apparatus of Claim 9, wherein at least one FET of the plurality of FETs is a Negative-type MOSFET (N-type MOSFET).

11. (Original) The apparatus of Claim 8, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

12. (Currently Amended) A method for current leakage correction for a leaky capacitor, wherein the leaky capacitor is connected to ground, comprising:

measuring voltage across the leaky capacitor;

providing the measured voltage to a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

providing a sustaining charge to the leaky capacitor.

13. (Original) The method of Claim 12, wherein the step of providing the measured voltage to a scaled capacitor further comprises utilizing a plurality of current mirrors with an adjusted width and length to provide the measured voltage to the scaled capacitor.

14. (Currently Amended) A computer program product for current leakage correction for a leaky capacitor in a computer system, wherein the leaky capacitor is connected to ground, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for measuring voltage across the leaky capacitor;

computer code for providing the measured voltage to a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

computer code for providing a sustaining charge to the leaky capacitor.

15. (Original) The computer program product of Claim 14, wherein the computer code for providing the measured voltage to a scaled capacitor further comprises computer code for

utilizing a plurality of current mirrors with an adjusted width and length to provide the measured voltage to the scaled capacitor.

16. (Currently Amended) A circuit for current leakage correction coupled to a leaky capacitor, wherein the leaky capacitor is connected to ground, comprising:

a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

a plurality of current mirrors, wherein the plurality of current mirrors further comprise:

at least one first current mirror is at least configured to be coupled to the leaky capacitor; and

at least one second current mirror is at least configured to be coupled to the scaled capacitor that is at least configured to provide a potential difference across the scaled capacitor that is substantially equal to a potential difference across the leaky capacitor minus the potential difference across the at least one second current mirror.

17. (Original) The circuit of Claim 16, wherein the plurality of current mirror further comprises a plurality of transistors.

18. (Original) The circuit of Claim 16, wherein the plurality of current mirrors further comprises a plurality of Field Effect Transistors (FET).

19. (Original) The circuit of Claim 18, wherein at least one FET of the plurality of FETs is a Positive-Channel FET (PFET), wherein the PFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

20. (Original) The circuit of Claim 19, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

21. (Original) The circuit of Claim 18, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

22. (Original) The circuit of Claim 16, wherein the plurality of current mirrors further comprise a plurality of bipolar transistors.

23. (Original) The circuit of Claim 16, wherein the plurality of current mirrors further comprise a plurality of Metal-Oxide Semiconductor FETs (MOSFETs).

24. (Original) The circuit of Claim 23, wherein at least one MOSFET of the plurality of MOSFETs is a Positive-type MOSFET (P-type MOSFET), wherein the P-type MOSFET is at least configured to inject current into the leaky capacitor to compensate for a current leak.

25. (Original) The circuit of Claim 24, wherein at least one FET of the plurality of FETs is a Negative-type MOSFET (N-type MOSFET).

26. (Original) The circuit of Claim 23, wherein at least one FET of the plurality of FETs is a Negative-Channel FET (NFET).

27. (New) An apparatus for current leakage correction coupled to a leaky capacitor, wherein the leaky capacitor is connected to ground and a current source that is in a non-conducting high impedance state, comprising:

a scaled capacitor, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the leaky capacitor; and

a plurality of current mirrors, wherein the plurality of current mirrors further comprise:

at least one first current mirror is at least configured to be coupled to the leaky capacitor;

at least one second current mirror is at least configured to be coupled to the scaled capacitor that is at least configured to provide a potential difference across the scaled capacitor that is equal to a potential difference across the leaky capacitor minus the potential difference across the at least one second current mirror;

wherein the at least one first current mirror further comprises at least one transistor that is at least configured to inject current into the leaky capacitor; and

wherein the at least one second current mirror further comprises at least two paired transistors in parallel that are at least configured to apply current leakage compensation.